UNITED STATES PATENT APPLICATION

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FOR

METHOD OF FABRICATING A THIN FILM TRANSISTOR AND MANUFACTURING EQUIPMENT

This application claims the benefit of Korean Patent Application No. 2000-26788, filed on May 18, 2000, the entirety of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a thin film transistor (TFT), and more particularly, to a TFT having an organic gate-insulating layer.

Discussion of the Related Art

A thin film transistor (TFT) is generally used as a switching device. For example, a liquid crystal display (LCD) device widely adopts the TFT for its switching device. Since the TFT is relatively easy to form on large, relatively inexpensive, glass substrates, the TFT is one of the most focused-on devices.

LCDs are based on the optical anisotropy of a liquid crystal (LC). A LC has long, thin molecules whose orientational alignment can be controlled by an applied electric field. When the alignment of the LC molecules is appropriately controlled, an applied light is refracted along the alignment direction of the LC molecules such that an image is displayed.

Active matrix (AM) LCDs, in which thin film transistors (TFTs) and pixel electrodes are arranged in an array matrix, are typically used because of their high resolution and superiority in displaying moving images. In an AM LCD, each TFT serves as a switch for a corresponding pixel. A "switched on" pixel transmits incident light.

In an off state of a TFT, the TFT serves to prevent a cross talk between closely spaced unit pixels and serves to extend a period of a signal applied to a liquid crystal layer.

Figure 1 is a cross-sectional view illustrating a conventional LCD panel 20. As shown, the LCD panel has lower and upper substrates 2 and 4, and an interposed liquid crystal layer 10. The lower substrate 2 includes a substrate 1, a TFT "S" as a switching element to selectively change the orientation of the liquid crystal molecules, and a pixel electrode 14 for the application of a voltage that produces an electric field across the liquid crystal layer 10 in accordance with signals from the TFT "S". The upper substrate 4 has a color filter 8 for providing color. A common electrode 12 is formed on the color filter 8. The common electrode 12 together with the pixel electrode produces the electric field across the liquid crystal layer 10. The pixel electrode 14 is arranged over a pixel portion "P", i.e., a display area. Further, to prevent leakage of the liquid crystal layer 10 between the substrates 2 and 4, the substrates 2 and 4 are sealed by a sealant 6. The nematic, smectic, and cholesteric liquid crystals are most widely used in the above-mentioned LCD panel.

sub a1 > When an electric signal is applied to the gate electrode 26 of the TFT "S", a data signal can be applied to the pixel electrode 14. Thus, unless the electric signal is applied to the gate electrode, a data signal cannot be applied to the pixel electrode 14

A design specification for the lower substrate usually depends on materials and needed specification for the various elements mentioned above. For example, when fabricating a large (such as SXGA and UXGA) LCD device, the resistance of the gate line material can be a critical factor in determining the quality of the LCD device. Therefore, a highly conductive metal, such as aluminum (Al) or an aluminum alloy, is usually used for the gate lines of large LCD devices.

In practice, an inverted staggered type TFT is widely employed due to its advantages of simplicity and high quality. The inverted staggered type TFT can be classified as either a back-channel-etch type or an etching-stopper type, based on the method of forming a channel. As the back-channel-etch type has a simpler structure, a structure of the back-channel-etch type TFTs is shown.

FIG. 2 is a cross-sectional view illustrating a back-channel-etch type TFT used for a typical LCD device. As shown, a gate electrode 30 is formed on a substrate 1, and a gate-insulating layer 32 is formed to cover the gate electrode 30. An active layer 34 is formed on the gate-insulating layer 32, and an ohmic contact layer 36 is formed on the active layer 34. In addition, source and drain electrodes 38 and 40 are formed on the ohmic contact layer 36. The source and drain electrodes 38 and 40 respectively overlap first and second edge portions of the gate electrode 30.

Aluminum (Al) is widely used for the gate electrode 30 because it has a low resistance that reduces RC delays. However, pure aluminum often produces hillocks that can cause defects. Therefore, an aluminum alloy (or an aluminum layer that is covered by another metal such as a refactory metal, for example) is usually used instead of pure aluminum. The source and drain electrodes 38 and 40 are usually made of chromium (Cr) or molybdenum (Mo).

The gate-insulating layer 32 is usually made of silicon nitride (SiN_x) or silicon oxide (SiO_2), each of which can be deposited at a relatively low temperature (e.g., below 350°C) and has a superior insulating property. The active layer 34 is usually an amorphous silicon layer (a-Si:H), which also can be deposited at a relatively low temperature.

To form the ohmic contact layer 36, a dopant ion is doped into a portion of the active layer 34. Specifically, a gas having Group III or Group V atoms such as phosphorous (P) or boron (B) is used for the above-mentioned ion dopant. A typical LCD device usually adopts a phosphorous doped amorphous silicon layer (n^+ a-Si:H) for the ohmic contact layer 36. When the phosphorous doping is applied, for example, PH_3 doping gas including phosphorous (P) is used.

As explained above, a typical TFT used for an LCD device is formed by depositing not only metal layers including the gate electrode 30 but also silicon layers including the gate-insulating layer 32, active layer 34, and ohmic contact layer 36. The gate-insulating layer 32, active layer 34, and ohmic contact layer 36 are deposited using the same deposition equipment, for example, a plasma enhanced chemical vapor deposition system (PECVD).

In case of the gate-insulating layer 32, after a mixture of gas including NH_3, N_2, and SiH_4 gases is allowed into the PECVD system, the mixture of gas is decomposed under a plasma condition. Then, a silicon nitride (SiN_x) film is formed from the decomposed mixture gas such that the gate-insulating layer 32 is achieved.

For the active layer 34, after the above-mentioned NH_3 and N_2 gases are discharged from the PECVD system, H_2 gas is additionally introduced. Then, the above-mentioned SiH_4 gas and H_2 gas are used together to form a pure amorphous silicon layer (a-Si:H), the active layer 32. In addition, to form the ohmic contact layer 36, a small quantity of PH_3 doping gas is further added to the mixture of SiH_4 and H_2 gases in the PECVD system. Then, the phosphorous doped amorphous silicon layer (n^+ a-Si:H) for the ohmic contact layer 36 is formed from the mixture of SiH_4, H_2 ,and PH_3 gases.

For the above-mentioned thin film transistor "S", silicon nitride (SiN_X) is used as the gate-insulating layer 32. However, when the gate-insulating layer 32 is silicon nitride (SiN_X), a parasitic capacitance "C" is present between the gate electrode 30 and the source electrode 38, and between the gate electrode 30 and the drain electrode 40. Since silicon nitride generally has a dielectric constant of about 6, the above-mentioned parasitic capacitance "C" has some (non-negligible) effect on the display quality of the LCD device.

In addition, for a high resolution LCD device, the gate electrode (gate line) is preferred to be thick or wide such that the gate electrode (gate line) has a lower resistance. Since a wide gate electrode (gate line) causes poor aperture ratio, a thick gate electrode (gate line) is preferred over the wide one. However, a thick gate electrode (gate line) may cause a break in the gate-insulating layer.

To avoid the above-mentioned problem of the thick gate electrode, an organic gate-insulating layer has been recently researched and developed. For a typical organic gate-insulating layer, benzocyclobutene (BCB) used for a passivation layer of a typical LCD device is usually used. Since BCB has a dielectric constant of below 3, it causes a smaller parasitic capacitance than silicon nitride which has a dielectric constant of about 6. In addition, since BCB has a superior flatness, it is suitable for the gate-insulating layer to cover the thick gate electrode.

FIG. 3 is a cross-sectional view illustrating a TFT having a BCB gate-insulating layer 33. As shown, even with a gate electrode 30, the BCB gate-insulating layer 33 provides a flat surface. Because of the flat surface of the BCB gate-insulating layer 33, source and drain electrodes 38 and 40 as well as the active layer 34 on the BCB gate-insulating layer 33 are formed to have proper shapes.

FIG. 4 is a block diagram illustrating a conventional process for forming the above-mentioned BCB gate-insulating layer. At first, BCB is deposited on a substrate having a gate electrode. Since BCB remains liquid under atmospheric conditions, it must be cured after be deposited. Curing of BCB is usually performed under nitrogen gas (N_2) atmosphere in a heated oven. Since nitrogen gas is an inert gas, the above-mentioned nitrogen gas (N_2) atmosphere prevents BCB from combining with oxygen gas (O_2). After curing, an active layer is formed in a vacuum equipment. Then, source and drain electrodes are formed in a later process.

For the above-mentioned conventional process for forming the BCB gate-insulating layer, the substrate having a BCB film is in an atmospheric condition during a transfer from the heat oven to the vacuum equipment, after curing. In that case, atmospheric oxygen gas may combine with the surface of the BCB film, or contaminants in the atmosphere may be attached to the surface thereof such that the BCB film is contaminated. If the BCB film has a contaminated surface, an interface property between the BCB gate-insulating layer and the active layer is deteriorated. Returning to FIG. 3, an interface "F" between the gate-insulating layer 33 and active layer 34 directly affects an on-current property of the TFT "S". As mentioned above, if the interface "F" is poor, the electric characteristices of the TFT "S" deteriorats. Returning to FIG. 4 illustrating the conventional process, the BCB film is present in the atmosphere during a transfer between the curing of the BCB film and the forming of the active layer. Then, the surface of the BCB film is contaminated such that the BCB gate-insulating layer made of the BCB film and the active layer which will be formed later have a poor interface property therebetween.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a method of fabricating a thin film transistor and manufacturing equipment that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method of fabricating a thin film transistor including an organic gate-insulating layer having an improved interface property.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, A method of fabricating a thin film transistor, the method comprising forming a gate electrode of the thin film transistor on a substrate; depositing an organic insulating layer over the substrate having the gate electrode; transferring the substrate to a heating and deposition equipment; heating the substrate in the equipment under vacuum and curing the organic insulating layer; and forming a silicon layer on the organic insulating layer in the equipment without breaking the vacuum.

In another aspect of the prensent invention, an apparatus for fabricating a thin film transistor, wherein the thin film transistor includes an organic insulating layer and an active layer having a first amorphous silicon layer and a doped amorphous silicon layer over a substrate, the apparatus comprising a first reaction chamber for curing the organic insulating

layer; a second reaction chamber for forming the first amorphous silicon layer; a third reaction chamber for forming the doped amorphous silicon layer; and a preparation chamber for providing a vacuum condition, wherein the preparation chamber is adjacent the first, second and third reaction chambers and the substrate is transferred from the first chamber to the second chamber under the vacuum condition through the preparation chamber.

In another aspect of the present invention, an apparatus for fabricating a transistor, wherein the transistor includes an organic layer and a semiconductor layer, the apparatus comprising a first chamber for curing the organic layer; a second chamber for forming the semiconductor layer; and a preparation chamber adjacent the first and second chambers, wherein the preparation chamber allows a product being formed into the transistor to transfer between the first and second chambers under vacuum.

In another aspect of the present invention, A method of making a liquid crystal display device having a first substrate and a second substrate, the method comprising forming a gate electrode on the first substrate; forming an organic layer over the first substrate having the gate electrode; curing the organic layer in a first chamber; transferring the first substrate having the organic layer from the first chamber to a second chamber without exposing the first substrate having the organic layer to oxygen atmosphere during transfer; forming an active layer on the organic layer in the second chamber; forming source and drain electrodes on the active layer; forming a pixel electrode connected to the drain electrode; and forming a liquid crystal layer between the first substrate and the second substrate.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide a further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

FIG. 1 is a cross-sectional view illustrating a liquid crystal display device according to the related art;

FIG. 2 is a cross-sectional view illustrating a typical back-channel-etch type TFT used for an LCD device;

FIG. 3 is a cross-sectional view illustrating a TFT having a typical BCB gate-insulating layer;

FIG. 4 is a block diagram illustrating a conventional process for forming the BCB gate-insulating layer of the TFT shown in FIG. 3;

FIG. 5 is a plan view illustrating a vacuum equipment according to the preferred embodiment of the present invention; and

FIG. 6 is a block diagram illustrating a process for forming a BCB gate-insulating layer according to the preferred embodiment.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Reference will now be made in detail to the illustrated embodiments of the present invention, an example of which is shown in the accompanying drawings.

FIG. 5 illustrates a vacuum equipment 100, which is used for fabricating a BCB gate-insulating layer (reference 33 of FIG. 3) of a thin film transistor (reference "S" of FIG. 3), according to the preferred embodiment of the present invention. The inventive vacuum equipment 100 has a preparation chamber 50, which is unified with first to third reaction chambers 60, 70, and 80. The first reaction chamber 60 is used for curing the BCB gate-insulating layer, whereas the second and third reaction chambers 70 and 80 are used for forming an active layer. Each of the first to third reaction chambers 60 to 80 preferably has a heat plate (not shown) that controls a temperature of the reaction chamber. Each heat plate (not shown) of the first to third reaction chambers 60 to 80 serves to control a temperature of elements or layers fabricated in the corresponding reaction chamber.

When the elements are formed and sequentially moved from the first to third reaction chambers 60 to 80, a vacuum condition is maintained in the preparation chamber 50 of the vacuum equipment 100. Thus, the thin film transistor is always shielded from outside atmosphere during the fabricating process thereof.

FIG. 6 is a block diagram illustrating a fabricating process for the thin film transistor having the BCB gate-insulating layer according to the present invention. At first, an organic insulating layer, such as a BCB film, for the gate-insulating layer is deposited on a substrate (reference 1 of FIG. 3) having a gate electrode (reference 30 of FIG. 3). A spin coating or other suitable process is preferably used to deposit the BCB film on the substrate. Then, the substrate on which the BCB film is deposited, is transferred to the preparation chamber 50 of the vacuum equipment 100. While vacuum is maintained in the preparation chamber 50, the substrate is moved into the first reaction chamber 60. In the first reaction

chamber 60, the BCB film deposited on the substrate is cured at about 250 °C under an inert gas condition. Nitrogen gas (N_2) is preferably used as the inert gas.

After the curing of the BCB film is finished, the substrate is moved from the first reaction chamber 60 to the second reaction chamber 70, and then to the third reaction chamber 80 without breaking the vacuum. In the second and third reaction chamber 70 and 80, an active layer including a first (such as pure) silicon layer (not shown) and a second (such as doped) silicon layer (not shown) may be formed, respectively. After the above-mentioned first silicon layer and second silicon layer are formed, other elements such as source and drain electrodes (reference 38 and 40 of FIG. 3) are formed using known suitable fabricating processes thereof.

Instead of BCB other organic materials may be used for the gate insulating layer including acryl. A gate-insulating layer made of acryl film can be used as a gate-insulating layer covering the gate electrode on the substrate. The above-explained forming process is also suitable for the acryl gate-insulating layer.

As explained above, the curing of the organic film such as BCB film and the forming of an active layer are performed under vacuum. Since the organic film is shielded from outside atmosphere during the curing, the interface between the organic film and the active layer improves.

In addition, to fabricate the thin film transistor having the organic gate-insulating layer such as BCB, the present invention preferably uses a vacuum equipment 100 where the first to third reaction chambers 60 to 80 and the preparation chamber 50 are an integrated unit or combined as one unit. The preparation chamber 50 serves to provide a vacuum condition such that the substrate having various elements of the thin film transistor

on fabrication are transferred in and out of the reaction chambers under the vacuum condition. The first reaction chamber 60 preferably serves as a heating oven to cure the organic film, and the second and third reaction chambers 70 and 80 preferably serve to deposit the first silicon layer and the second silicon layer, respectively. Thus, a heating oven and a silicon deposition apparatus are unified together in the vacuum equipment 100. The first reaction chamber 60 serves as the heating oven, whereas the second and third reaction chambers 70 and 80 serve as the silicon deposition apparatus.

It will be apparent to those skilled in the art that various modifications and variation can be made in the illustrated device and method without departing from the spirit or scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention that come within the scope of the appended claims and their equivalents.